## AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

**LISTING OF CLAIMS**

1. (Currently Amended) ~~An inverted-phase~~ A phase detector ~~for a circuit~~ that receives a clock signal and a delayed clock signal, comprising:

a reference circuit that outputs a reference signal; and

a feedback circuit that generates a feedback signal,

wherein said feedback signal is one of greater than and less than said reference signal when the clock signal changes state before the delayed clock signal, and

wherein said feedback signal is the other of greater than and less than said reference signal when the clock signal changes state after the delayed clock signal.

2. (Currently Amended) The ~~inverted-phase~~ phase detector of claim 1 further comprising a sense amplifier that communicates with said reference circuit and said feedback circuit and that generates one of an early signal and a late signal.

3. (Currently Amended) The ~~inverted-phase~~ phase detector of claim 2 further comprising a latch that communicates with said sense amplifier and that latches ~~said~~ an output of said sense amplifier.

4. (Currently Amended) The ~~inverted-phase~~ phase detector of claim 1 wherein said reference signal has a substantially constant voltage.

5. (Currently Amended) The ~~inverted-phase~~ phase detector of claim 1 wherein said ~~inverted-phase~~ phase detector has an accuracy that is less than 25 picoseconds.

6. (Currently Amended) The ~~inverted-phase~~ phase detector of claim 1 wherein said ~~inverted-phase~~ phase detector has an accuracy that is less than 5 picoseconds.

7. (Original) A phase adjustment system, comprising:

a clock circuit that outputs a clock signal and a delayed clock signal;

a reference circuit that outputs a reference signal;

an feedback circuit that generates a feedback signal based on said clock signal and said delayed clock signal,

wherein said feedback signal is one of greater and less than said reference signal when said clock signal changes state before said delayed clock signal, and

wherein said feedback signal is the other of greater than and less than said reference signal when said clock signal changes state after said delayed clock signal;

a phase correction control circuit that adjusts a phase of at least one of said clock signal and said delayed clock signal based on said feedback signal and said reference signal.

8. (Original) The phase adjustment system of claim 7 wherein said phase correction control circuit includes a sense amplifier that communicates with said reference circuit and said feedback circuit and that generates one of an early signal and a late signal.

9. (Currently Amended) The phase adjustment system of claim 8 wherein said phase correction control circuit includes a latch that communicates with said sense amplifier and that latches ~~said~~ an output of said sense amplifier.

10. (Original) The phase adjustment system of claim 7 wherein said reference signal has a substantially constant voltage.

11. (Original) The phase adjustment system of claim 7 wherein said inverted-phase detector has an accuracy that is less than 25 picoseconds.

12. (Original) The phase adjustment system of claim 7 wherein said inverted-phase detector has an accuracy that is less than 5 picoseconds.

13. (Currently Amended) ~~An inverted-phase~~ A phase detector that receives a clock signal and a delayed clock signal, comprising:

reference means for providing a reference signal; and

feedback means for generating a feedback signal based on the clock signal and the delayed clock signal,

wherein said feedback signal is one of greater than and less than said reference signal when the clock signal changes state before the delayed clock signal, and

wherein said feedback signal is the other of greater than and less than said reference signal when the clock signal changes state after the delayed clock signal.

14. (Currently Amended) The ~~inverted-phase~~ phase detector of claim 13 further comprising sense means that communicates with said reference means and said feedback means for generating one of an early signal and a late signal.

15. (Currently Amended) The ~~inverted-phase~~ phase detector of claim 14 further comprising latch means that communicates with said sense means for latching ~~said~~ an output of said sense means.

16. (Currently Amended) The ~~inverted-phase~~ phase detector of claim 13 wherein said reference signal has a substantially constant voltage.

17. (Currently Amended) The ~~inverted-phase~~ phase detector of claim 13 wherein said ~~inverted-phase~~ phase detector has an accuracy that is less than 25 picoseconds.

18. (Currently Amended) The ~~inverted-phase~~ phase detector of claim 13 wherein said ~~inverted-phase~~ phase detector has an accuracy that is less than 5 picoseconds.

19. (Original) A phase adjustment system, comprising:

clock means that outputs a clock signal and a delayed clock signal;

reference means for providing a reference signal;

feedback means that receives said clock signal and said delayed clock signal for generating a feedback signal,

wherein said feedback signal is one of greater and less than said reference signal when said clock signal changes state before said delayed clock signal, and

wherein said feedback signal is the other of greater than and less than said reference signal when said clock signal changes state after said delayed clock signal; and

phase correction control means for adjusting at least one of a phase of said clock signal and said delayed clock signal based on said feedback signal and said reference signal.

20. (Original) The phase adjustment system of claim 19 wherein said phase correction control means includes sense means that communicates with said reference means and said feedback means for generating one of an early signal and a late signal.

21. (Currently Amended) The phase adjustment system of claim 20 wherein said phase correction control means includes latch means that communicates with said sense means for latching ~~said~~ an output of said sense means.

22. (Original) The phase adjustment system of claim 19 wherein said reference signal has a substantially constant voltage.

23. (Original) The phase adjustment system of claim 19 wherein said inverted-phase detector has an accuracy that is less than 25 picoseconds.

24. (Original) The phase adjustment system of claim 19 wherein said inverted-phase detector has an accuracy that is less than 5 picoseconds.

25. (Currently Amended) A method for operating ~~an inverted-phase~~ a phase detector that receives a clock signal and a delayed clock signal, comprising:

generating a reference signal; and

generating a feedback signal,

wherein said feedback signal is one of greater than and less than said reference signal when the clock signal changes state before the delayed clock signal, and

wherein said feedback signal is the other of greater than and less than said reference signal when the clock signal changes state after the delayed clock signal.

26. (Original) The method of claim 25 further comprising generating one of an early signal and a late signal.

27. (Original) The method of claim 26 further comprising latching said one of said early signal and said late signal.

28. (Original) The method of claim 25 wherein said reference signal has a substantially constant voltage.

29. (Currently Amended) The method of claim 25 wherein said ~~inverted-phase~~ phase detector has an accuracy that is less than 25 picoseconds.

30. (Currently Amended) The method of claim 25 wherein said ~~inverted-phase~~ phase detector has an accuracy that is less than 5 picoseconds.

31. (Original) A method for operating a phase adjustment system, comprising:

generating a clock signal and a delayed clock signal;

providing a reference signal;

generating a feedback signal based on said clock signal and said delayed clock signal,

wherein said feedback signal is one of greater and less than said reference signal when said clock signal changes state before said delayed clock signal, and

wherein said feedback signal is the other of greater than and less than said reference signal when said clock signal changes state after said delayed clock signal; and

adjusting a phase of at least one of said clock signal and said delayed clock signal based on said feedback signal and said reference signal.

32. (Original) The method of claim 31 further comprising generating one of an early signal and a late signal.

33. (Original) The method of claim 32 further comprising latching said one of said early signal and said late signal.

34. (Original) The method of claim 31 wherein said reference signal has a substantially constant voltage.

35. (Currently Amended) The method of claim 31 wherein said ~~inverted-phase~~ phase detector has an accuracy that is less than 25 picoseconds.

36. (Currently Amended) The method of claim 31 wherein said ~~inverted-phase~~ phase detector has an accuracy that is less than 5 picoseconds.